OPTICAL READER HAVING REDUCED PARAMETER DETERMINATION DELAY

Field of the Invention

The present invention relates to optical readers in general and in particular to a method for reducing a parameter determination delay of an optical reader.

Background of the Prior Art

Prior to commencing comprehensive image data processing, which may include e.g. searching for symbol or character representations, decoding and character recognition processing, presently available optical readers clock out and capture in a memory location at least one exposure test frame of image data, read pixel data from the memory-stored exposure test frame to determine an exposure parameter value that is based on actual illumination conditions, then utilize the exposure parameter value in the exposure of a frame of image data that is clocked out, and then subjected to searching, decoding, and/or character recognition processing. The frame of image data exposed utilizing the exposure parameter based on actual illumination conditions is not available for reading until after it is clocked out. Presently available optical readers therefore exhibit an appreciable inherent exposure parameter determination delay. Readers having higher

resolution imagers have slower frame clock out rates and therefore longer exposure parameter determination delays.

There is a growing demand for higher resolution optical readers, including optical readers that incorporate mega pixel image sensors. Accordingly, there is growing need to address the parameter determination delay problem associated with presently available optical readers.

Summary of the Invention

According to its major aspects and broadly stated, the present invention is a method for controlling an optical reader to reduce the reader's parameter determination delay. According to the invention, an image sensor is adapted to clock out image data from an image sensor according to two modes of operation, a "low resolution" clock out mode of operation and a "normal resolution" clock out mode of operation.

In a low resolution mode, some pixels of the reader's image sensor pixel array are clocked out at a normal clock out speed sufficient to develop electrical signals that accurately represent the intensity of light incident on the pixel array, while other pixels of the array are either not clocked out or are clocked out at a higher clock out rate which is

insufficient to allow development of electrical signals that accurately represent the intensity of light at the respective pixels but which nevertheless, result in an increase in the overall frame clock out rate of the frame of image data. In a normal resolution mode of operation the image sensor is caused to clock out electrical signals corresponding to each pixel of the array at a constant "normal mode" speed which is a speed sufficient to ensure that the electrical signal corresponding to each pixel accurately represents the intensity of light incident on the pixel.

An optical reader according to the invention operates an image sensor in a low resolution mode of operation in order to clock out and capture a parameter-determining frame of image data at high speed, reads pixel data from the parameter determination frame to determine an operation parameter based on actual illumination conditions, then utilizes the operation parameter in operating an image sensor according to high resolution mode in the clocking out of a succeeding frame of image data that is captured and subjected to comprehensive image data processing which may include image data searching, decoding, and/or recognition processing. Clocking out some of the pixels of an array at high speed during execution of the low resolution mode significantly decreases the reader's

parameter determination delay.

These parameters determined by reading pixel values from a low resolution parameter determination frame of image data according to the invention may include an exposure time parameter, an amplification parameter for controlling amplification of an electrical signal prior to its analog to digital conversion, an illumination level parameter (intensity or period of illumination), a dark or light level adjustment parameter and an analog-to-digital converter reference voltage parameter for adjusting the high and/or low reference voltages of the reader's analog to digital converter.

These and other details, advantages and benefits of the present invention will become apparent from the detailed description of the preferred embodiment hereinbelow.

Brief Description of the Drawings

Figs. 1a and 1b are image maps illustrating possible low resolution frames of image data clock out during a low resolution frame clock out mode of the invention;

Fig. 2a is a block diagram of an optical reader of a type in which the invention may be incorporated;

Figs. 2b-2h show various types of optical reader housings in which the invention may be incorporated;

Fig. 3a is a process flow diagram illustrating frame clocking operations in an optical reader having an image sensor including a one-frame buffer.

Fig. 3b is a time line illustrating frame clock out operations in a prior art optical reader;

Fig. 3c is a time line illustrating a frame clock out of operations in an optical reader operated according to the invention.

Detailed Description of the Invention

When operated to generate valid pixel data, presently available optical reading devices clock out electrical signals corresponding to pixel positions of an image sensor at a uniform clock out rate such that the electrical signal corresponding to each pixel of the image sensor array accurately represents light incident on the pixel.

By contrast, an image sensor of the present invention is made to operate under two major frame capture modes, a "low resolution" frame clock out mode and a "normal resolution" frame clock out mode. In a "low resolution" mode of operation, an image sensor according to the invention is operated to clock out electrical signals corresponding to some pixels of an image sensor array at a high clock out rate and

other pixels of the image sensor at a normal clock out rate. Clocking out a portion of the electrical signals using a faster than normal clock out rate results in a reduction in the overall frame clock out time while clocking out a portion of the signals at a normal clock out rate enables the generation of pixel data sufficient to enable determination of parameter settings for use in subsequent frame captures. In a "normal resolution" mode of operation the image sensor is operated to clock out electrical signals corresponding to pixels of the array using a single uniform clock out speed as in prior art readers. The low resolution mode of operation may also be carried out by clocking out electrical signals corresponding to only a portion of a frame's pixels and not clocking out electrical signals corresponding to the remaining pixels.

A reader configured in accordance with the invention clocks out and captures in a memory storage location at least one parameter determination frame of image data in a "low resolution" frame capture mode, reads pixels of the parameter determination frame in establishing at least one operation parameter that is based on actual illumination conditions, utilizes the determined operation parameter in clocking out a subsequent frame of image data in a "normal resolution mode,"

then captures and subjects the frame of image data clocked out utilizing the operation parameter to image data searching, decoding, and/or recognition processing.

An optical reading system is which the invention may be employed is described with reference to the block diagram of Fig. 2a.

Optical reader 10 includes an illumination assembly 20 for illuminating a target object T, such as a 1D or 2D bar code symbol, and an imaging assembly 30 for receiving an image of object T and generating an electrical output signal indicative of the data optically encoded therein. Illumination assembly 20 may, for example, include an illumination source assembly 22, together with an illuminating optics assembly 24, such as one or more lenses, diffusers, wedges, reflectors or a combination of such elements, for directing light from light source 22 in the direction of a target object T. Illumination assembly 20 may comprise, for example, laser or light emitting diodes (LEDs) such as white LEDs or red LEDs. Illumination assembly 20 may include target illumination and optics for projecting an aiming pattern 27 on target T. Illumination assembly 20 may be eliminated if ambient light levels are certain to be high enough to allow high quality images of object T to be taken. Imaging assembly

30 may include an image sensor 32, such as a 1D or 2D CCD, CMOS, NMOS, PMOS, CID OR CMD solid state image sensor, together with an imaging optics assembly 34 for receiving and focusing an image of object T onto image sensor 32. The array-based imaging assembly shown in Fig. 2a may be replaced by a laser array based imaging assembly comprising multiple laser sources, a scanning mechanism, emit and receive optics, at least one photodetector and accompanying signal processing circuitry.

Optical reader 10 of Fig. 2a also includes programmable control circuit 40 which preferably comprises an integrated circuit microprocessor 42 and an application specific integrated circuit (ASIC 44). The function of ASIC 44 could also be provided by field programable gate array (FPGA). Processor 42 and ASIC 44 are both programmable control devices which are able to receive, output and process data in accordance with a stored program stored in memory unit 45 which may comprise such memory elements as a read/write random access memory or RAM 46 and an erasable read only memory or EROM 47. RAM 46 typically includes at least one volatile memory device but may include one or more long term non-volatile memory devices. Processor 42 and ASIC 44 are also both connected to a common bus 48 through which program data

and working data, including address data, may be received and transmitted in either direction to any circuitry that is also connected thereto. Processor 42 and ASIC 44 differ from one another, however, in how they are made and how they are used.

More particularly, processor 42 is preferably a general purpose, off-the-shelf VLSI integrated circuit microprocessor which has overall control of the circuitry of Fig. 2a, but which devotes most of its time to decoding image data stored in RAM 46 in accordance with program data stored in EROM 47. Processor 44, on the other hand, is preferably a special purpose VLSI integrated circuit, such as a programmable logic or gate array, which is programmed to devote its time to functions other than decoding image data, and thereby relieve processor 42 from the burden of performing these functions.

The actual division of labor between processors 42 and 44 will naturally depend on the type of off-the-shelf microprocessors that are available, the type of image sensor which is used, the rate at which image data is output by imaging assembly 30, etc. There is nothing in principle, however, that requires that any particular division of labor be made between processors 42 and 44, or even that such a division be made at all. This is because special purpose processor 44 may be eliminated entirely if general purpose

processor 42 is fast enough and powerful enough to perform all of the functions contemplated by the present invention. It will, therefore, be understood that neither the number of processors used, nor the division of labor there between, is of any fundamental significance for purposes of the present invention.

With processor architectures of the type shown in Fig. 2a, a typical division of labor between processors 42 and 44 will be as follows. Processor 42 is preferably devoted primarily to such tasks as decoding image data, once such data has been stored in RAM 46, recognizing characters represented in stored image data according to an optical character recognition (OCR) scheme, handling menuing options and reprogramming functions, processing commands and data received from control/data input unit 39 which may comprise such elements as trigger 74 and keyboard 78 and providing overall system level coordination.

Processor 44 is preferably devoted primarily to controlling the image acquisition process, the A/D conversion process and the storage of image data, including the ability to access memories 46 and 47 via a DMA channel. Processor 44 may also perform many timing and communication operations. Processor 44 may, for example, control the illumination of

LEDs 22, the timing of image sensor 32 and an analog-to-digital (A/D) converter 36, the transmission and reception of data to and from a processor external to reader 10, through an RS-232, a network such as an ethernet, a serial bus such as USB, a wireless communication link (or other) compatible I/O interface 37. Processor 44 may also control the outputting of user perceptible data via an output device 38, such as a beeper, a good read LED and/or a display monitor which may be provided by a liquid crystal display such as display 82. Control of output, display and I/O functions may also be shared between processors 42 and 44, as suggested by bus driver I/O and output/display devices 37' and 38' or may be duplicated, as suggested by microprocessor serial I/O ports 42A and 42B and I/O and display devices 37" and 38'. As explained earlier, the specifics of this division of labor is of no significance to the present invention.

Figures 2b through 2g show examples of types of housings in which the present invention may be incorporated. Figs. 2b-2g show 1D/2D optical readers 10-1, 10-2 and 10-3. Housing 12 of each of the optical readers 10-1 through 10-3 is adapted to be graspable by a human hand and has incorporated therein at least one trigger switch 74 for activating image capture and decoding and/or image capture and character recognition

operations. Readers 10-1 and 10-2 include hard-wired communication links 79 for communication with external devices such as other data collection devices or a host processor, while reader 10-3 includes an antenna 80 for providing wireless communication device or a host processor.

In addition to the above elements, readers 10-2 and 10-3 each include a display 82 for displaying information to a user and a keyboard 78 for enabling a user to input commands and data into the reader.

Any one of the readers described with reference to Figs. 2b through 2g may be mounted in a stationary position as is illustrated in Fig. 2h showing a generic optical reader 10 docked in a scan stand 90. Scan stand 90 adapts portable optical reader 10 for presentation mode scanning. In a presentation mode, reader 10 is held in a stationary position and an indicia bearing article is moved across the field of view of reader 10.

As will become clear from the ensuing description, the invention need not be incorporated in a portable optical reader. The invention may also be incorporated, for example, in association with a control circuit for controlling a non-portable fixed mount imaging assembly that captures image data representing image information formed on articles transported

by an assembly line, or manually transported across a checkout counter at a retail point of sale location. Further, in portable embodiments of the invention, the reader need not be hand held. The reader may be part or wholly hand worn, finger worn, waist worn or head worn for example.

Referring again to particular aspects of the invention, a low resolution frame clock out mode of the invention is described in detail with reference to the pixel maps of Figs. 1a and 1b. Control circuit 40 establishes a clock out rate for clocking out an electrical signal corresponding to a pixel of an image sensor 32 by appropriate state control of control signals in communication with image sensor 32. In the present invention, image sensor 32 is selected to be of a type whose pixel clock out rate can be varied by way of control signals received from control circuit 40. In presently available optical readers, an image sensor's pixel clock out rate is not changed during the course of clocking out of a frame of image data.

In a "low resolution" frame clock out mode of the invention, however, control circuit 40 causes image sensor 32 to clock out electrical signals corresponding to the pixels of the array at least two speeds during a single frame capture period. During a single frame clock out period, control

circuit 40 controls image sensor 32 so that some pixels are clocked out at normal clock out rate sufficient to develop electrical signals accurately representing the intensity of light at the respective pixel positions, while other pixels are either not clocked out or are clocked out at a clock out rate which may be insufficient to allow development of electrical signals that accurately represent the intensity of light at the respective pixels but which nevertheless results in a reduction of the overall frame clock out time of the frame of image data being clocked out.

Fig. 1a shows a schematic diagram of an exemplary image map frame that is clocked out according to the low resolution frame clock out mode of the invention and then captured into memory 45. The image map is divided into "zones" of valid data and invalid data. Valid zones 84 shown are rows of pixels that are clocked out at a normal clock out speed while invalid zones 86 shown are rows of pixel that are clocked out at a faster clock out speed, which is normally (but not necessarily) a speed insufficient to allow development of electrical signals accurately representing the intensity of light at a pixel.

Fig. 1b shows another possible division of an image map into valid zones and invalid zones. This type of embodiment

in which valid zones 84 comprise less than full pixel rows is conveniently realized by appropriate control of an image sensor manufactured using CMOS fabrication methods. Using CMOS fabrication methods, an image sensor can be merged with a microprocessor, an ASIC, or another timing device on a single die to the end that a preestablished clocking sequence in which a pixel clock out rate is changed multiple times during the course of clock out a frame of image data may be actuated in response to the activation of a single control signal in communication with image sensor 32.

Using CMOS fabrication techniques, image sensors are readily made so that electrical signals corresponding to certain pixels of a sensor can be selectively clocked out without clocking out electrical signals corresponding to remaining pixels of the sensor. CMOS image sensors are available from such manufacturers as Symagery, Pixel Cam, Omni Vision, Sharp, Natural Semiconductor, Toshiba, Hewlett-Packard and Mitsubishi. Further aspects of a partial frame clock out mode are described in commonly assigned application Serial No._ _____ entitled "Optical Reader Having Partial Frame Operating Mode" filed concurrently herewith and incorporated herein by reference.

The invention is also conveniently realized with use of

an image sensor having an image sensor discharge function. Image sensors having a discharge function are typically adapted to receive a discharge clock out signal which when active results in all pixels of a frame being read out at a high clock out rate insufficient to allow development of electrical signals. In presently available readers having a directional function, a control circuit sets the discharge clocking signal to an active state while clocking out an initial "discharge period" frame of image data immediately after reception of a trigger actuation. This initial discharge process removes any residual charges built up on image sensor 32 prior to capturing a first frame including valid pixel data.

For producing an image map divided into valid and invalid zones using an image sensor having a discharge function, control circuit 40 may be made to intermittently change the state of a discharge clock out signal during a frame clock out period during which image sensor 32 is otherwise operated according to a normal resolution clock out mode.

An exemplary embodiment of the invention in which the invention is employed in a reader equipped with a SONY ICX084AL CCD image sensor (that includes a one frame analog buffer memory) and a SONY CXD2434TQ timing generator is

described with reference to Figs. 3a, 3b and 3c. Fig. 3a shows a flow diagram, of an imaging system in which the image sensor includes a one frame buffer memory. For purposes of illustrating the advantages of the invention, Fig. 3b shows a time line illustrating the time required to clock out and capture a frame of image data useful for searching and decoding in a prior art reader having a buffer memory not configured to operate in accordance with a low resolution frame clock out mode. Fig. 3c shows a time line illustrating the time required to clock out and capture a frame of image data useful for searching, decoding, and recognizing characters in a reader having a buffer memory configured to operate in a low resolution frame clock out mode according to the invention.

When a reader includes a one frame buffer memory, then the activation of an appropriate frame clock out signal by image sensor 32 causes electrical charges representative of light on pixels of an image sensor's pixel array 32a to be transferred to analog buffer memory 32b and causes electrical signals corresponding to pixel value storage locations of buffer 32b (representing light on the pixels during a previous timing period) to be clocked out to analog to digital converter 36 so that the frame of image data stored on buffer

memory can be captured in memory 45, wherein the data may be read by control circuit 40.

Referring to time line 92 corresponding a prior art reader it can be seen that a substantial parameter determination delay is present without use of a low resolution frame capture mode according to the invention. At time T0, control circuit 40 activates a frame discharge control signal so that residual charges built up in the storage locations of buffer memory 32b are eliminated or "cleaned" during clock out period CPO.

At time T1, control circuit 40 activates a frame clocking signal to commence the clock out a first frame of pixel data according to a normal resolution frame clock out mode(the pixel data clocked out during clock out period CP1 is normally invalid pixel data). During clock out period CP1, the charges built up on pixel array 32a during clock out period CP0 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP1 pixel array 32a is exposed to light for a time determined by an exposure parameter value, e_0, that was previously transmitted at time Te_0 prior to time T1. The exposure parameter e_0 is based on previous exposure values during a previous trigger actuation period or based on expected illumination conditions, but is

not based on actual illumination conditions present.

At time T2, control circuit 40 activates a frame clock out signal to commence the clock out of a second frame of image data in accordance with a normal resolution frame clock out mode. During clock out period CP2, the charges built up on pixel array 32a during clock out period CP1 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP2 pixel array 32 is exposed to light for a time determined by an exposure parameter value, e_1, that was previously transmitted at time Te_1 prior to time T2. The exposure parameter e_1, like exposure parameter e_0, also cannot be based on actual illumination conditions since the most recent frame image data available for reading by circuit 40 prior to the transmittal of exposure parameter e_1 is the invalid frame data resulting from transmittal of frame discharge signal at time T0.

At time T3, control circuit 40 activates a frame clock out signal to commence the capture of a third frame of image data in accordance with a normal resolution frame clock out mode. During clock out period CP3, the charges built up on pixel array 32a during clock out period CP2 are transferred to buffer memory 32b and then clocked out to A/D converter 36. Also during clock out period CP3, pixel array 32a is exposed

to light for a time determined by an exposure parameter value, e_2, that was previously transmitted at time Te_2 prior to time T3. Unlike the previous exposure values e_0 and e_1, the exposure parameter value e_2 can be a value determined from actual illumination conditions since the frame of image data resulting from pixel array 32a being exposed to light during clock out period CP1, is available for reading by control circuit 40 prior to the time that the exposure parameter e_2 must be communicated to image sensor 32. However, because of the built in one frame delay resulting from the presence of buffer 32b, it is seen that a frame of image data clocked out while being exposed with the exposure parameter value e_2, determined based on actual illumination conditions, will not be available for reading by control circuit unit after the expiration of clocking period CP4. Accordingly, it can be seen that the above reader exhibits a typical parameter determination delay of four normal resolution clock out periods, CP1+CP2+CP3+CP4 plus the frame discharge clock out parameter CP0. The normal resolution frame clock out rate of the above-referenced SONY image sensor is about 33.37 ms and the frame discharge rate is about 8.33 ms, resulting in a typical-case total parameter determination delay in the example described of 140ms (an earlier frame may be subjected

to image data searching, decoding, and recognition if e_0 or e_1 yields an image of acceptable quality).

Advantages of operating image sensor 32 according to a low resolution frame clock out mode of operation are easily observable with reference to time line 94 corresponding to a reader having an image sensor operated in accordance with a low resolution frame clock out mode. In the example illustrated by time line 94 control circuit 40 operates image sensor as described in connection with Fig. 3b except that control circuit 40 operates image sensor 32 according to a low resolution frame clock out mode during clocking periods CP1, CP2, and CP3. Because electrical signals corresponding to only some of the pixels during these timing periods are clocked out at speeds sufficiently slow to read valid image data, the total frame clock out time association with these clocking periods is significantly shorter than that of a frame clocked out according to a normal resolution frame clock out mode. In an exemplary embodiment in which control circuit 40 alternatingly changes the state of a discharge clock out control signal (known as an EFS signal) in communication with a SONY ICX084AL CCD image sensor, to result in a zone division pattern having valid zones comprising four pixel rows clocked out at normal speed bounded by invalid rows having eighteen

rows of pixels clock out at high speed, the low resolution frame clock out rate is 8.52 ms. The overall typical parameter determination delay is therefore reduced to T0+T1+T2+T3+T4=66.2 ms as compared to the 140 ms delay in the prior art reader example described with reference to Fig. 3a.

In the example described in which image sensor 32 comprises a one frame buffer 32b, pixel array 32a is exposed to light for at least some time currently as electrical signals are clocked out from buffer 32b. In the control of presently available image sensors that do not have one frame buffers, frame clock out periods normally follow frame exposure periods without overlapping the exposure periods.

A low resolution parameter determination frame of image data clocked out using a low resolution clock out mode is useful for determining an exposure control parameter because exposure parameter values can be accurately determined by sampling only a small percentage of pixel values from a frame of image data. In fact, for improving the processing speed of an optical reader it is preferred to determine an exposure control value based on a sampling of a small percentage of pixel values from a frame of image data. The proper exposure parameter setting varies substantially linearly with illumination conditions, and therefore is readily determined based on a sampling of pixel values from a single frame of

image data.

Additional reader operating parameters can be determined by reading pixel values from a frame of image data clocked out according to a low resolution clock out mode of the invention. These additional parameters which may be determined from a low resolution parameter determining frame of image data include an amplification parameter for adjusting the gain of an amplifier prior to analog-to-digital conversion, an illumination level parameter for adjusting the current level delivered to, and therefore the radiance of light emitted from LEDs 22, an illumination time parameter for adjusting the on-time of LEDs 22, a light level parameter for adjusting a light level of a subsequently captured frame of image data, a dark level parameter for adjusting a dark level, of a subsequently captured frame of image data, and an analog-to digital converter reference parameter for adjusting a reference voltage of analog-to-digital converter 36.

While the present invention has been explained with reference to the structure disclosed herein, it is not confined to the details set forth and this invention is intended to cover any modifications and changes as may come within the scope of the following claims: